

## **INFORMATION DISCLOSURE STATEMENT A**

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FORM PTO-1449 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO.	SERIAL NO.
				TI-12592A.23	10/816,076
<b>LIST OF DOCUMENTS CITED BY APPLICANT</b> <i>(Use several sheets if necessary)</i>					
<b>APPLICANT</b> Hashimoto, et al.					
		FILING DATE	GROUP		
		March 31, 2004	2188		
<b>OTHER DOCUMENTS</b> <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>					
<p>Bell Laboratories, Incorporated, <u>Transmission Systems for Communications</u>, 5th Edition, 1982, pp. 590-591.</p> <p>Cole, Bernard C., "Motorola's Radical SRAM Design Speeds Systems 40%", <u>Electronics</u>, July 23, 1987, pp. 66-68.</p> <p>Hashimoto, Masashi et al., "A 20-ns 256K X 4 FIFO Memory", <u>IEEE Journal of Solid-State Circuits</u>, Vol. 23, No. 2, April 1988, pp. 490-499.</p> <p>Hashimoto, Masashi et al., "A 20 ns 256K X 4 FIFO Memory", <u>IEEE 1987 Custom Integrated Circuits Conference</u>, May 4-7, 1987, pp. 315-318.</p> <p>Horowitz, Mark et al., "MIPS-X: A 20-MIPS Peak, 32-bit Microprocessor with On-Chip Cache", <u>IEEE Journal of Solid-Circuits</u>, Vol. SC-22, No. 5, October 1987, pp. 790-799.</p> <p>Lineback, J. Robert, "System Snags Shouldn't Slow the Boom in Fast Static RAMS", <u>Electronics</u>, July 23, 1987, pp. 60-62.</p> <p>Miyaguchi et al., "A Field Store System With Single 1Mbit Field Memory", <u>IEEE Transactions on Consumer Electronics</u>, Vol. 34, No. 3, August 1988, pp. 397-401.</p> <p>Morris, S. Brent et al., "Processes for Random and Sequential Accessing in Dynamic Memories", <u>IEEE Transactions on Computers</u>, Vol. C-28, No. 3, March 1979, pages 225-237.</p> <p>Motorola, :16Kx4 Bit Synchronous Statis RAM with Output Registers and Output Enable", Motorola Semiconductor Technical Data, MCM6293.</p> <p>Motorola, "16Kx4 Bit Synchronous Statis RAM with Output Registers and Output Enable", Motorola Semiconductor Technical Data, MCM6294.</p> <p>Nakagawa et al., "A 1 Mb Field Memory For TV Pictures", <u>IEEE 1987 Custom Integrated circuits Conference</u>, Pages 319-322.</p> <p>Ohara, Kazuhiro et al., "A Field Store System With Single 1Mbit Field Memory, ICCE Digest of Technical Papers", pages 70-71, June, 1988.</p> <p>Wada, R. et al., "A Color Television Receiver With Digital Frame Memory", <u>1966 IEEE Transactions on Consumer Electronics</u>, Vol. 4, No. 3, pages 128-129.</p>					
EXAMINER		DATE CONSIDERED 1/10/05			

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## **INFORMATION DISCLOSURE STATEMENT B**

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## **INFORMATION DISCLOSURE STATEMENT B**

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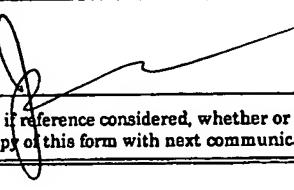
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U.S. PATENT DOCUMENTS					
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	3,740,723	06/1973	Beausoleil et al	395	425
	3,758,761	09/1973	Henrion	371	8.1
	3,771,145	11/1973	Wiener	365	240
	3,821,715	06/1974	Hoff et al.	340	173
	3,882,470	05/1975	Hunter	364	200
	3,924,241	12/1975	Kronies	395	425
	3,969,706	07/1976	Proebsting et al.	365	189.02
	3,972,028	07/1976	Weber et al.	395	425
	3,975,714	08/1976	Weber et al.	395	800
	3,983,537	09/1976	Parsons et al.	395	425
	4,007,452	02/1977	Hoff	365	63
	4,038,648	07/1977	Chesley	365	201
	4,099,231	07/1978	Kotok et al.	395	425
	4,191,996	03/1980	Chesley	395	425
	4,205,373	05/1980	Shah	395	425
	4,247,817	01/1981	Heller	307	354
	4,249,247	02/1981	Patel	395	425
	4,286,321	08/1981	Baker et al.	364	200
	4,306,298	12/1981	McElroy	395	425
	4,315,308	02/1982	Jackson	364	200
	4,333,142	06/1982	Chesley	395	500
	4,355,376	10/1982	Gould	365	200
	4,373,183	02/1983	Means et al.	395	400
	4,385,350	05/1983	Hansen et al.	365	229
	4,443,864	04/1984	McElroy	395	325
	4,449,207	05/1984	Kung et al.	365	189.02
	4,468,738	08/1984	Hansen et al.	395	325
	4,470,114	09/1984	Gerhold	395	325
	4,481,625	11/1984	Roberts et al.	370	85
	4,488,218	12/1984	Grimes	395	325
	4,500,905	02/1985	Shibata	357	68
	4,519,034	05/1985	Smith et al.	395	550
	4,595,923	06/1986	McFarland, Jr.	340	825.5
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		4,630,193	12/1986	Kris	395	325	
		4,646,270	02/1987	Voss	365	189.02	
		4,649,511	03/1987	Gdula	395	425	
		4,649,516	03/1987	Chung et al.	395	250	
		4,654,655	03/1987	Kowalski	340	825.5	
		4,706,166	11/1987	Go	361	403	
		4,719,627	01/1988	Peterson et al.	371	40.2	
		4,745,548	05/1988	Blahut	395	425	
		4,764,846	08/1988	Go	361	388	
		4,770,640	09/1988	Walter	439	69	
		4,779,089	10/1988	Theus	340	825.5	
		4,785,394	11/1988	Fischer	395	325	9/1986
		4,811,202	03/1989	Schabowski	395	325	10/1981
		4,818,985	04/1989	Ikeda	340	825.5	11/1987
		4,837,682	06/1989	Culler	395	325	4/1987
		4,860,198	08/1989	Takenaka	364	200	9/1985
		4,933,835	06/1990	Sachs et al.	364	200	1/1989
		4,975,763	12/1990	Baudouin et al.	357	74	3/1988
		5,023,488	06/1991	Gunning	307	475	3/1990
		5,179,670	01/1993	Farmwald et al.	395	325	12/1989
		5,319,755	06/1994	Farmwald et al.	395	325	4/1990
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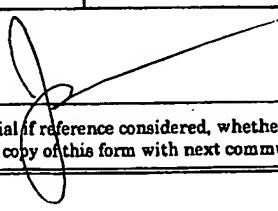
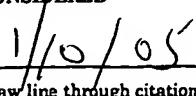
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				FILING DATE	GROUP
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<b>OTHER DOCUMENTS</b> <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>					
<p>Hawley, David, "Superfast Bus Supports Sophisticated Transactions," High Performance Systems, Sep. 1989.</p> <p>T. Yang, M. Horowitz, B. Wooley, "A 4-ns 4KX1-bit Two-Port BiCMOS SRAM," IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, pp. 1030-1040 (Oct. 1988).</p> <p>"Burndy Connects Advertisement," Electronic Engineering Times, pp. T24-T25 (Feb. 24, 1986).</p> <p>A. Kahn, "What's the Best Way to Minimize Memory Traffic," High Performance Systems, pp. 59-67 (Sep. 1989).</p> <p>N. Margulis, "Single Chip RISC CPU Eases System Design." High Performance Systems, pp. 34-36, 40-41, 44 (Sep. 1989).</p> <p>R. Matick, "Comparison of Memory Chip Organizations vs. Reliability in Virtual Memories," FTCS 12th Annual International Symposium Fault-Tolerant Computing, IEEE Computer Society Fault-Tolerant Technical Committee, pp. 223-227 (Jun. 22, 1982).</p> <p>Agarwal et al., "Scaleable Director Schemes for Cache Consistency," 15th Intern. Sump. Comp. Architecture, pp. 280-289 (Jun. 1988).</p> <p>Agarwal et al., "An Analytical Cache Model," ACM Trans. on Computer Systems, Vol. 7 No.2, pp. 184-215 (May 1989).</p> <p>Davidson, "Electrical Design of a High Speed Computer Package", IBM J. Res. Develop., Vol. 26, No. 3, pp. 349-361 (1982).</p> <p>Hart, "Multiple Chips Speed CPU Subsystems", High-Performance Systems, pp. 26-55 (Sep. 1989).</p> <p>Beresford, "How to Tame High Speed Design", High-Performance Systems, pp. 78-83 (Sep. 1989).</p> <p>Carson, "Advance On-Focal Plane Signal Processing for Non-Planar Infared Mosaics," SPIE, Vol. 311, pp. 53-58 (1981).</p> <p>Horowitz et al., "MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with ON-Chip Cache," IEEE J. Solid State Circuits, Vol. SC-22, No. 5, pp. 790-799 (Oct. 1987).</p> <p>Kwon et al., "Memory Chip Organizations for Improved Reliability in Virtual Memories," IBM Technical Disclosure Bulletin, Vol. 25, No. 6, November 1982, pp. 2952-2957.</p> <p>Pease et al., "Physical Limits to the Useful Packaging Density of Electronic Systems," IBM J. Res. Develop. Vol. 32 No. 5, (Sep. 1988).</p> <p>Peterson, "System-Level Concerns Set Performance Gains," High-Performance Systems, pp. 71-77 (Sep. 1989).</p>					
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<b>OTHER DOCUMENTS</b> <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>			
		Wooley et al., "Active Substrate System Integration," Private Communication, Semiconductor Research Corporation, 4 pages (Mar. 15, 1988).	
		H. Schumacher, "CMOS Subnanosecond True-ECL Output Buffer," IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, pp. 150-154 (Feb. 1990).	
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## **INFORMATION DISCLOSURE STATEMENT D**

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U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

**ATTY. DOCKET NO.**

SERIAL NO.

LIST OF DOCUMENTS CITED BY APPLICANT

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TI-12592A.23

10/816,076

**APPLICANT**

Hashimoto, et al.

FILING DATE

March 31, 2004 2188

## **U.S. PATENT DOCUMENTS**

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<p>Kimura et al., "Power Reduction Techniques in Megabit DRAM's", IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 3, June 1968.</p> <p>Nogami et al., "1-Mbit Virtually Static RAM, IEEE Journal of Solid-State Circuits", Vol. SC-21, No. 5, October 1986.</p> <p>Ohta et al., "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, October 1986.</p>					
<p>RECEIVED OCT 13 2004 U.S. PATENT AND TRADEMARK OFFICE</p>					
<p>EXAMINER</p> 					
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